High Accuracy Clock Synchronization Using IEEE 1588

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Outline

- **Motivation for this work**
- **Practical issues in achieving nanosecond level synchronization**
- **Experimental results**

Why would anyone want to sync to 1 ns?

Instrumentation and testing of high speed systems:

- **Electromagnetic signals propagate at ~1 foot/ns**
- **Network signaling rates in GHz range with packet dimensions in low ns range**

Agilent Labs Project Goals

Extend IEEE 1588 using

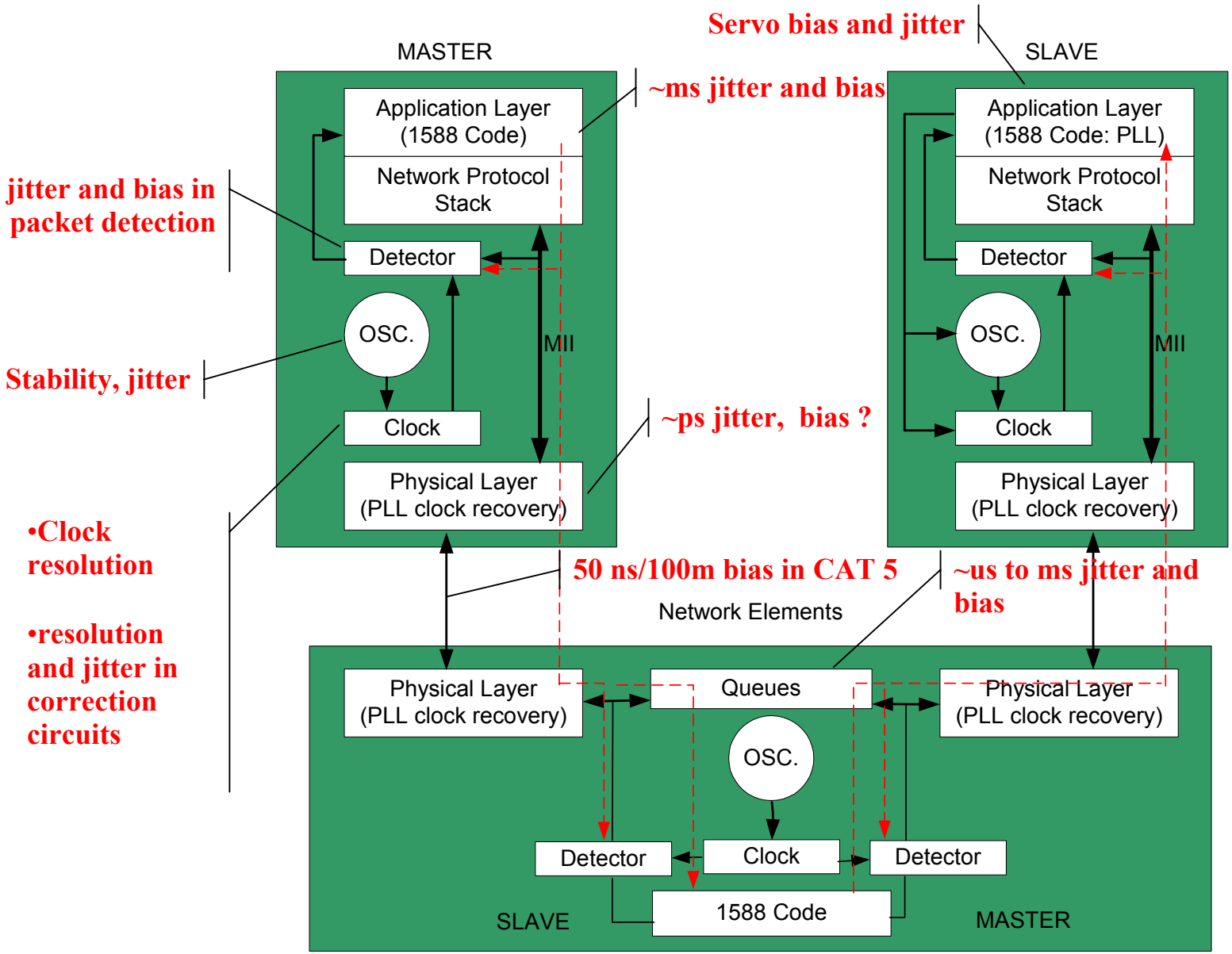
- More stable oscillators
- 100BT or Gigabit-Ethernet
- Increased bit resolution of clocks

Build demonstration version

Practical issues in achieving nanosecond level synchronization

- Background
- Oscillator characteristics
- Clock resolution
- Network signaling characteristics
- Topology

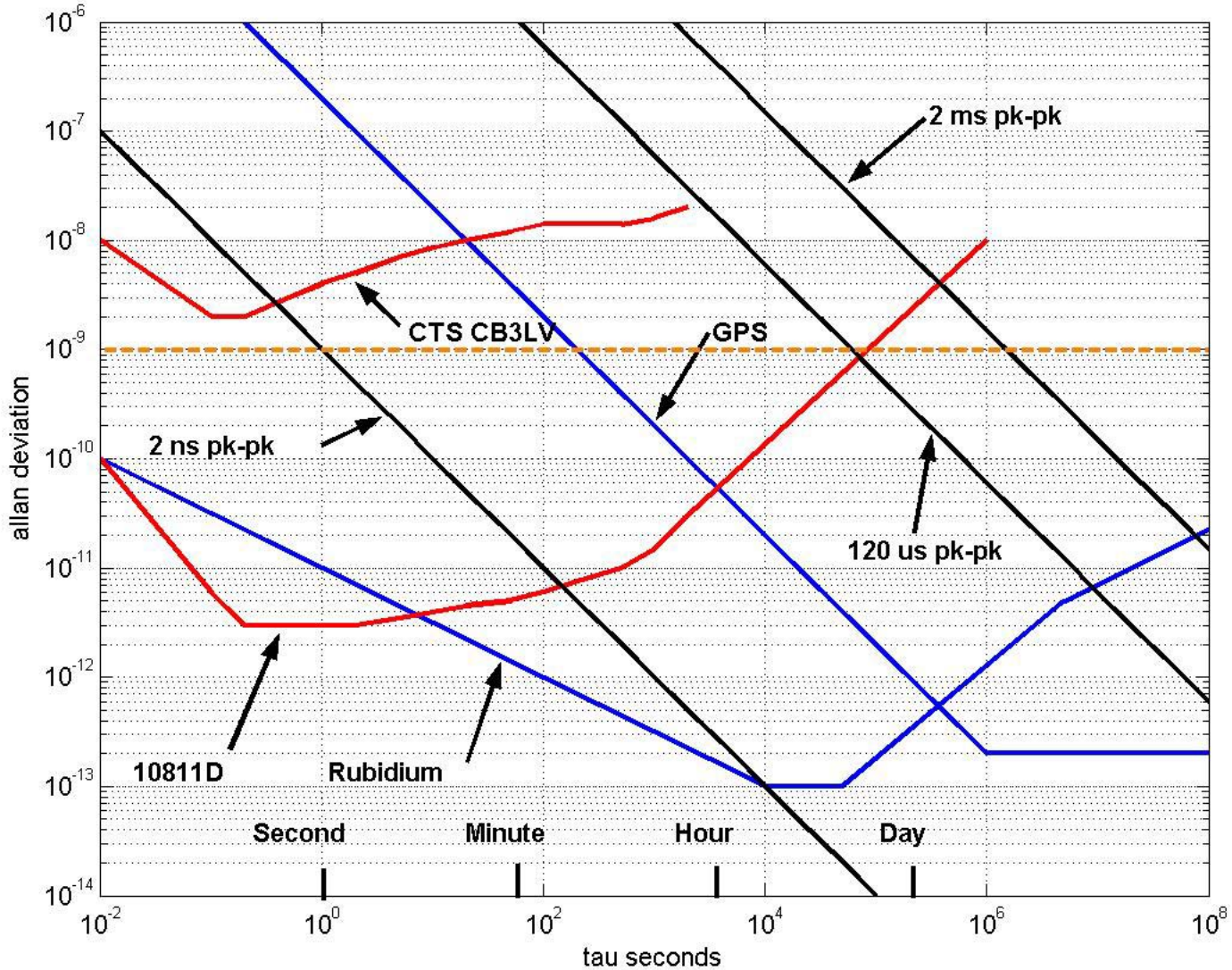
Background: High accuracy IEEE 1588 implementation



Thermal considerations

- **Oscillator drift is a major contributor to synchronization errors.**
- **Quartz crystal based oscillators**
  - **Uncompensated oscillators generally in few ppm/degree range**
  - **Thermal compensation typically x10 to x100 better**
- **Atomic based oscillators**
  - **Several orders of magnitude less drift than quartz**

Oscillators: Allan Deviations for Common Sources



Clock resolution considerations

- **The LSB of the actual clock and any datatype representation limits measurement and therefore synchronization accuracy**
- **The minimal rate and/or offset adjustment of the clock and any datatype representation limits the ability of the servo to correct to the desired accuracy.**

Network signaling characteristics

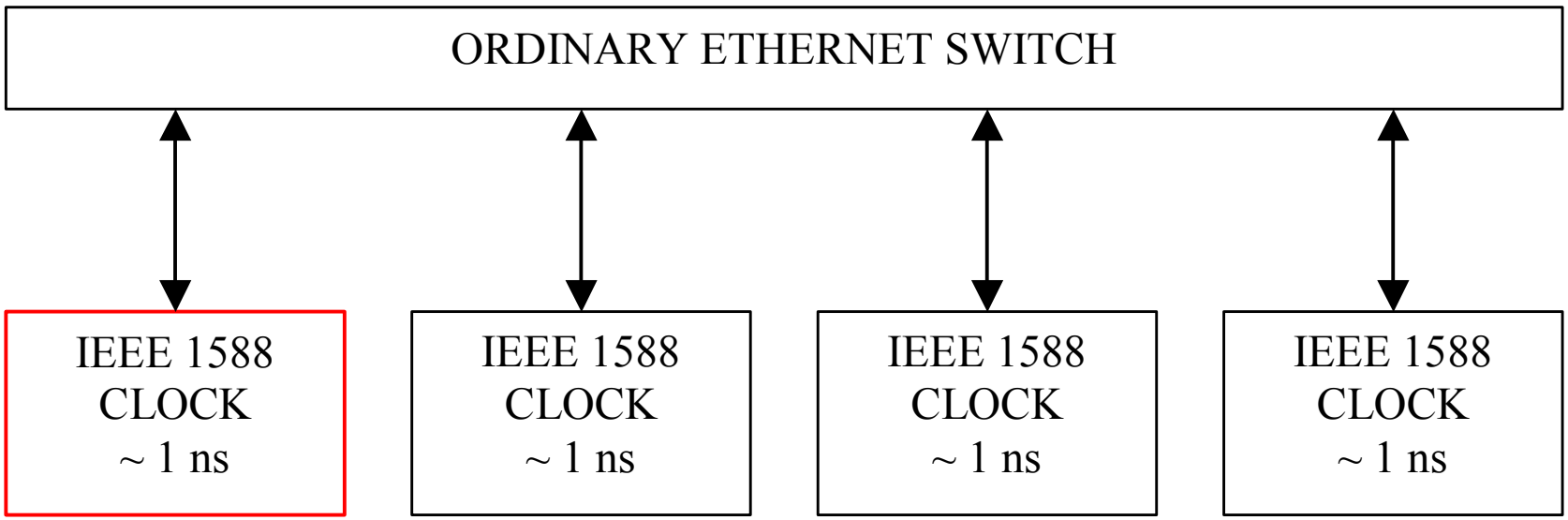
Signaling rates:

- **10 BT: 10 MHz, 100 ns period**
- **100 BT: 25 MHz, 40 ns period**
- **1000 BT: 125 MHz, 8 ns period**

Rise time of the network signal limits the accuracy of generating a reproducible time stamp

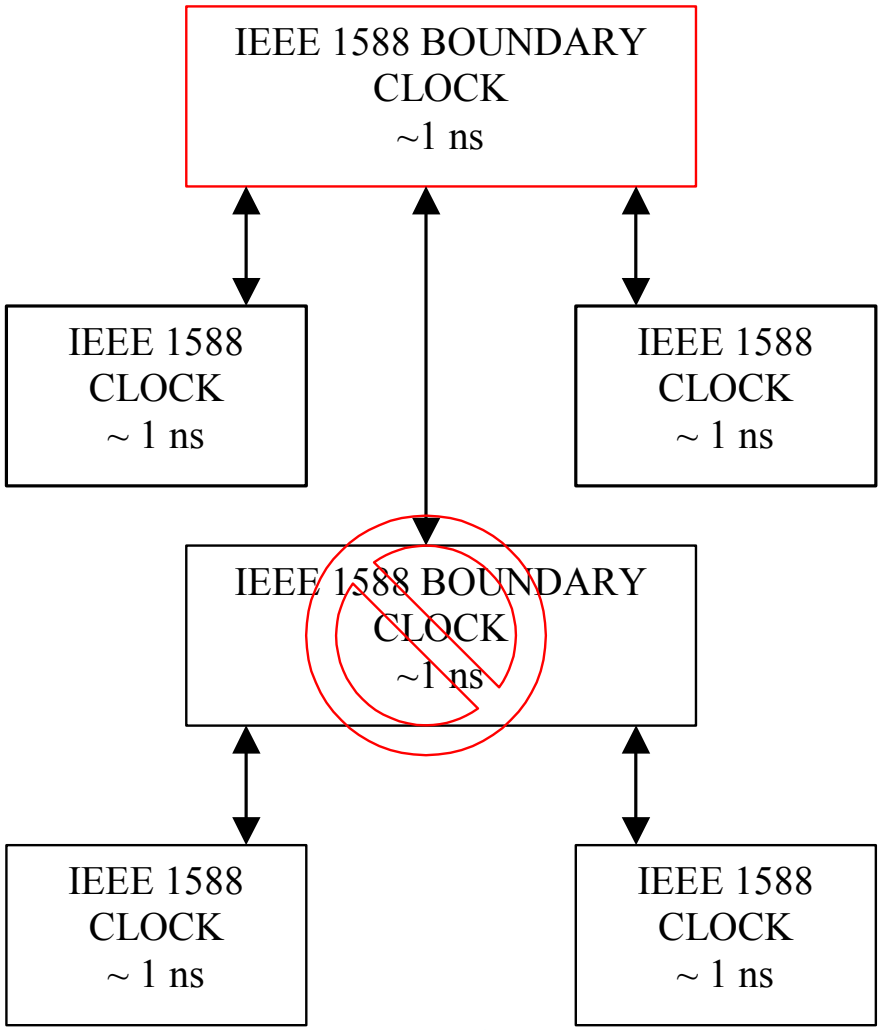
Accuracy Issues (topology)

Single subnet: switch jitter a problem at ns level



Accuracy Issues (topology)

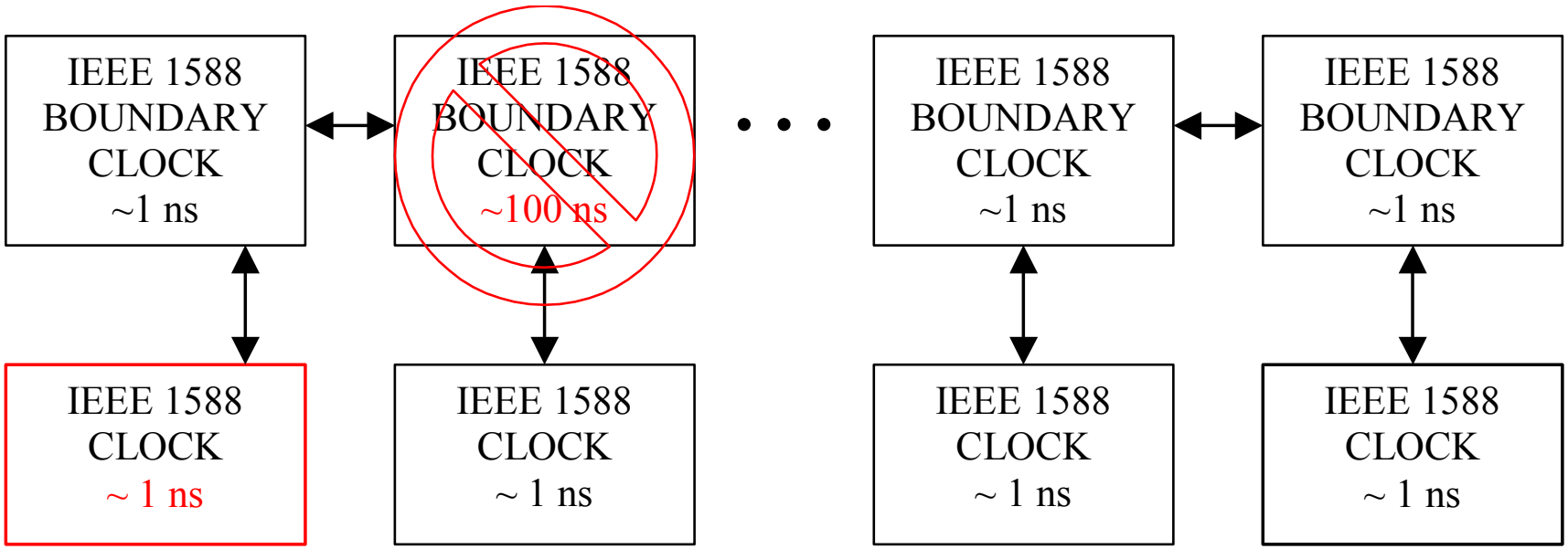
Hierarchy: Error accumulation at ns level



Accuracy Issues (topology)

Linear: not currently feasible at ns levels

1. **Cascaded devices accumulate servo error & quantization errors a severe problem at ns level**
2. **Low accuracy intermediate devices dominate error budget of chain**



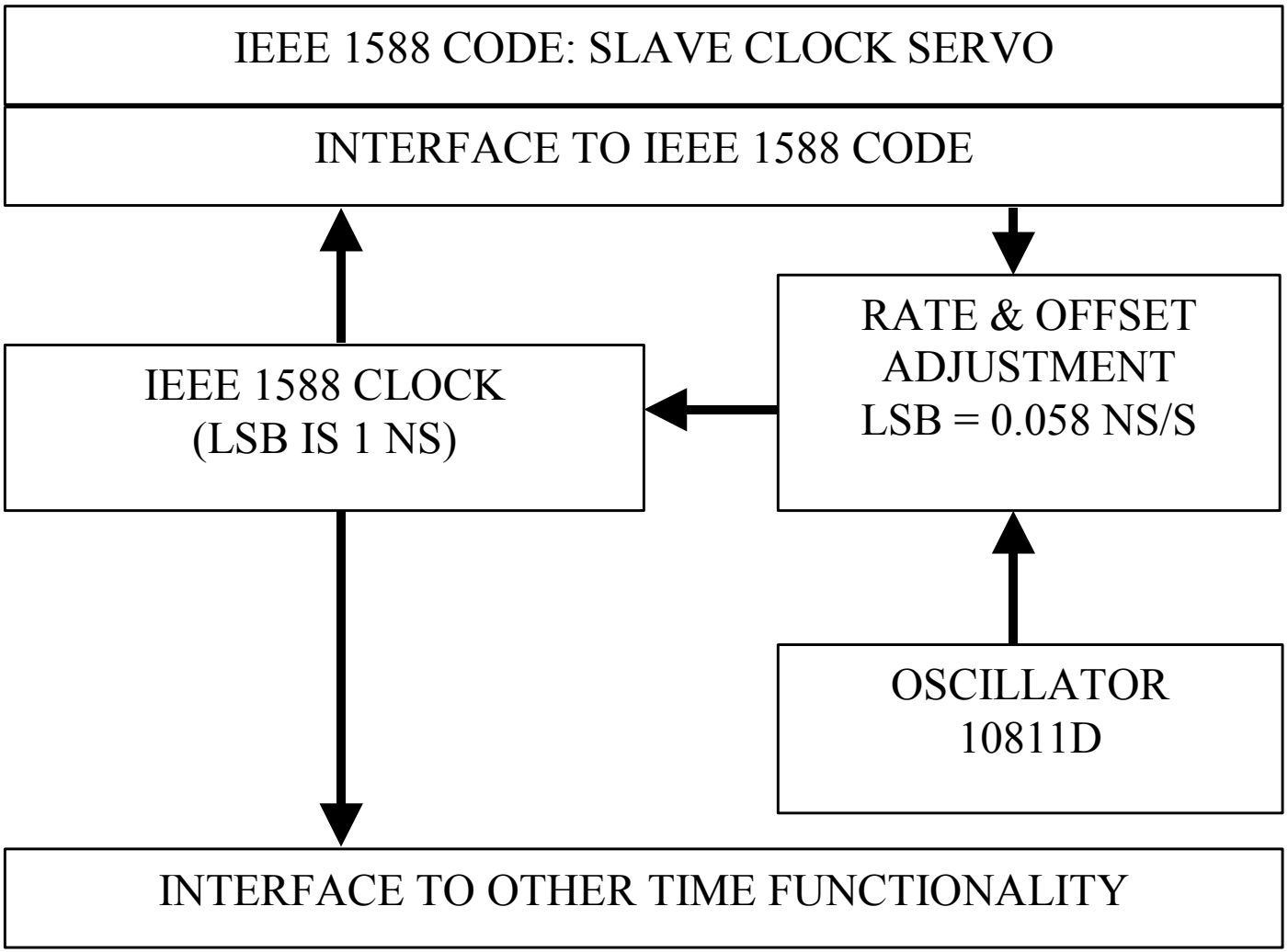
Accuracy Issues (asymmetry)

1. **Path asymmetry introduces offset errors significant at ns level**
2. **The major source of asymmetry in a complex network is queuing differences in switches/routers or in actual routing differences.**
   - **At ns level probably rules out all but single level hierarchy, i.e. direct master boundary clock to slave**
3. **Physical media can also be asymmetric**
   - **CAT5 cable asymmetry is nominally 25-50ns/100m**
   - **Measure and correct for delay**

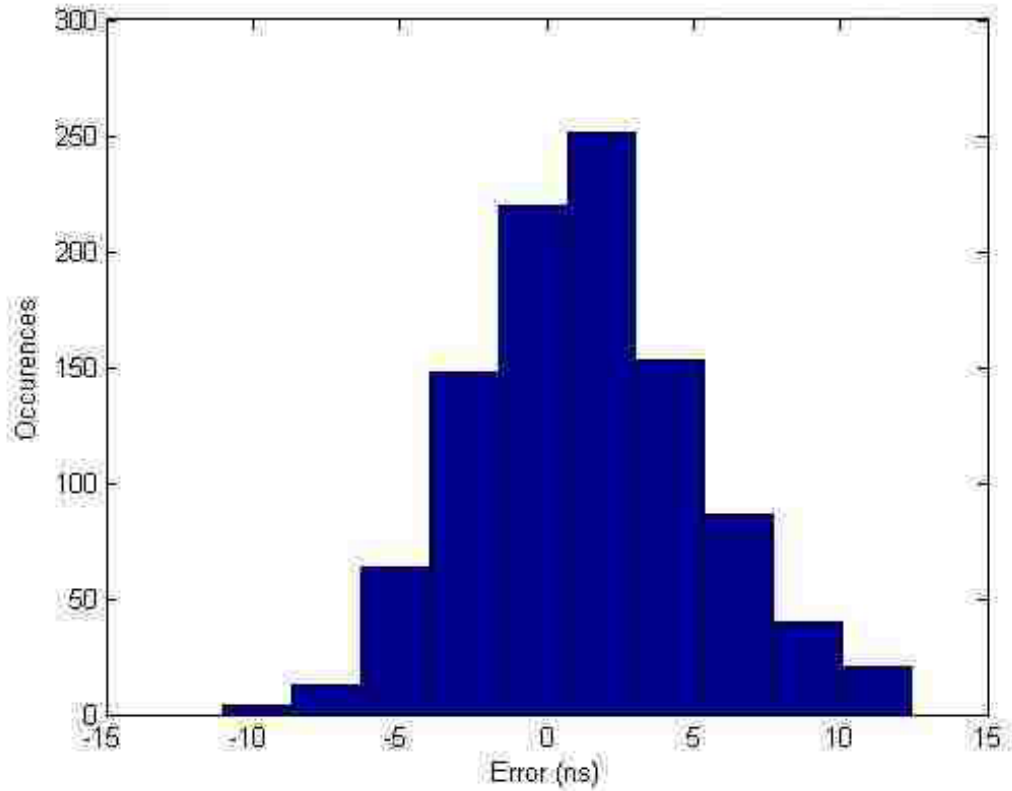
Experimental results

- Clock design
- Measurements

Experimental clock design



Histogram of 1 PPS deviations in directly connected clocks.



Resolution (LSB) = 4 ns. Sync interval 2 seconds. Short averaging time. Standard deviation = 4.4 ns, mean = 1.5 ns.

Next steps: 1 ns LSB, long averaging time in servo.